SY89112U

2.5/3.3V Low Jitter, Low Skew 1:12 LVPECL Fanout Buffer with 2:1 Input MUX and Internal Termination

General Description

The SY89112U is a low jitter, low skew, high-speed LVPECL 1:12 differential fanout buffer optimized for precision telecom and enterprise server distribution applications. The input includes a 2:1 MUX for clock switchover application. Unlike other multiplexers, this input includes a unique isolation design to minimize channel-to-channel crosstalk. The SY89112U distributes clock frequencies from DC to >2GHz guaranteed over temperature and voltage. The SY89112U incorporates a synchronous output enable (EN) so that the outputs will only be enabled/disabled when they are already in the LOW state. This reduces the chance of generating "runt" clock pulses.

The SY89112U differential input includes Micrel's unique, patent-pending 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV ($200mV_{pp}$) without any level shifting or termination resistor networks in the signal path. For AC-coupled input interface, an on-board output reference voltage (VREF-AC) is provided to bias the center-tap (VT) pin. The outputs are 800mV, 100K-compatible LVPECL with fast rise/fall times guaranteed to be less than 220ps.

The SY89112U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89112U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

Precision Edge®

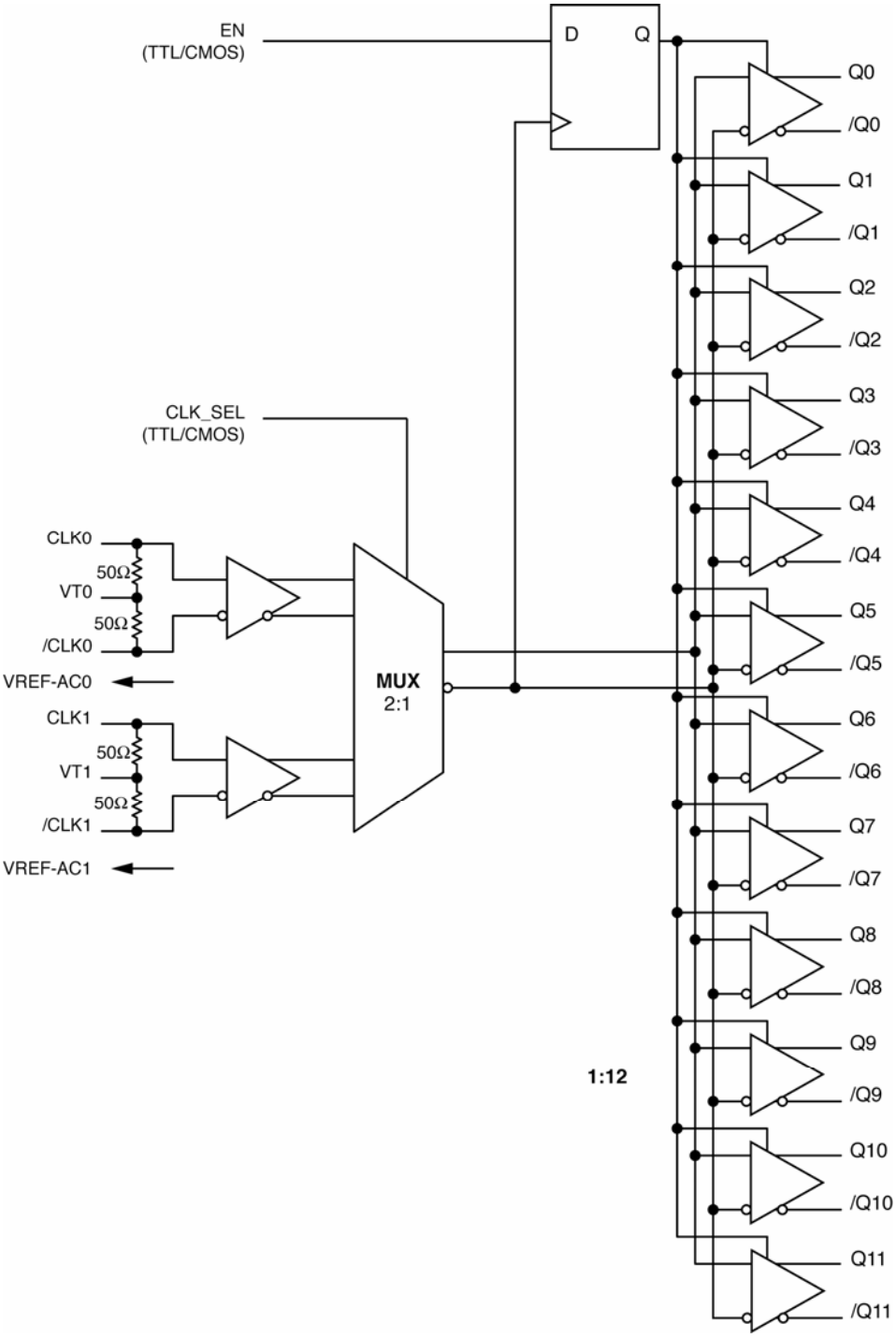
Features

- Selects between 1 of 2 inputs, and provides 12 precision, low skew LVPECL output copies
- Guaranteed AC performance over temperature and voltage:
  - DC to >2GHz throughput
  - <550ps propagation delay CLK-to-Q
  - <220ps rise/fall time
  - <25ps output-to-output skew
- Ultra-low jitter design:
  - $<1ps_{RMS}$ random jitter
  - $<10ps_{PP}$ total jitter (clock)
  - $<1ps_{RMS}$ cycle-to-cycle jitter
  - $<0.7ps_{RMS}$ crosstalk induced jitter
- Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-coupled differential inputs
- Unique, patent-pending 2:1 input MUX provides superior isolation to minimize channel-to-channel crosstalk
- 800mV, 100K LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range –40°C to +85°C
- Available in 44-pin (7mm x 7mm) MLF® package

Applications

- Multi-processor server
- SONET/SDH clock/data distribution
- Fibre Channel distribution
- Gigabit Ethernet clock distribution

Functional Block Diagram



hbwhelp@micrel.com or (408) 955-1690

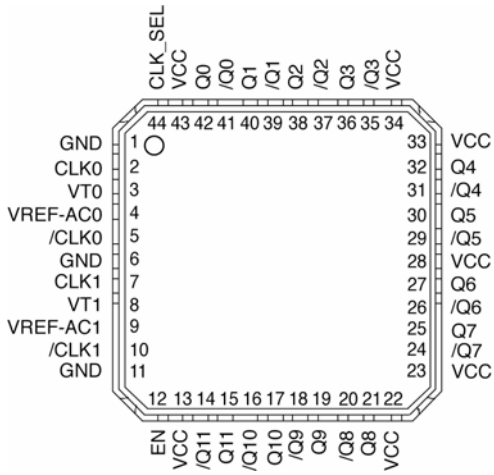
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89112UMI	MLF-44	Industrial	SY89112U	Sn-Pb
SY89112UMITR[2]	MLF-44	Industrial	SY89112U	Sn-Pb
SY89112UMY	MLF-44	Industrial	SY89112U with Pb-Free bar-line indicator	Matte-Sn Pb-Free
SY89112UMYTR[2]	MLF-44	Industrial	SY89112U with Pb-Free bar-line indicator	Matte-Sn Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



44-Pin MLF® (MLF-44)

Pin Description

Pin Number	Pin Name	Pin Function
2, 5 7, 10	CLK0, /CLK0 CLK1, /CLK1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
3, 8	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
4 9	VREF-AC0 VREF-AC1	Reference Voltage: These outputs bias to V_{CC}–1.2V. They are used when AC coupling the inputs (CLK, /CLK). For AC-coupled applications, connect V_{REF-AC} to the VT pin and bypass with a 0.01μF low ESR capacitor to V_{CC}. See "Input Interface Applications" section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
44	CLK_SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
12	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
13,22,23,28, 33,34,43	VCC	Positive power supply. Bypass with 0.1μF//0.01μF low ESR capacitors and place as close to each VCC pin as possible.
42, 41 40, 39 38, 37 36, 35 32, 31 30, 29 27, 26 25, 24 21, 20 19, 18 17, 16 15, 14	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4 Q5, /Q5 Q6, /Q6 Q7, /Q7 Q8, /Q8 Q9, /Q9 Q10, /Q10 Q11, /Q11	Differential 100K LVPECL Outputs: These LVPECL outputs are the precision, low skew copies of the inputs. Please refer to the truth table below for details. Unused output pairs may be left open. Terminate with 50Ω to V_{CC}–2V. See "LVPECL Output Interface Applications" section for more details.
1, 6, 11	GND, Exposed Pad	Ground. GND pins and exposed pad must both be connected to the most negative potential of chip the ground.

Truth Table

EN	CLK_SEL	Q	/Q
H	L	CLK0	/CLK0
H	H	CLK1	/CLK1
L	X	L(1)	H(1)

Note:

1. Transition occurs on next negative transition of the non-inverted input.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .....–0.5V to +4.0V
Input Voltage (V_{IN}) .....–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
Continuous 50mA
Surge..... 100mA
Termination Current
Source or sink current on VT ..... ±100mA
Input Current
Source or sink current on CLK, /CLK..... ±50mA
V_{REF-AC} Current
Source or sink current ..... ±2mA
Lead Temperature (soldering, 20 sec.) .....+260°C
Storage Temperature (T_s).....–65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC})..... +2.375V to +2.625V
.....+3.0V to +3.6V
Ambient Temperature (T_A)..... –40°C to +85°C
Package Thermal Resistance[3]
MLF® (θ_{JA})
Still-Air ..... 42°C/W
MLF® (ψ_{JB})
Junction-to-Board ..... 20°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375 3.0		2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}		95	130	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH} –0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN–/IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-VT (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVPECL Outputs DC Electrical Characteristics[5]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} – 2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics[5]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Note:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[6]

V_{CC} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC} – 2V, unless otherwise stated.

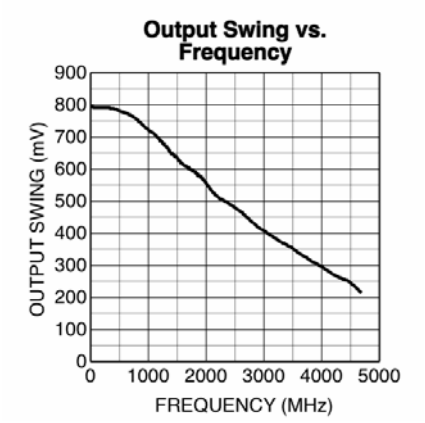
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 400mV	2	3		GHz
t_{PD}	Propagation Delay CLK to Q	V_{IN} ≥ 100mV	300	400	550	ps
	Propagation Delay CLK_SEL to Q		200	350	600	ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			150		fs/°C
t_S	Set-up Time EN-to-CLK	Note 7	0			ps
t_H	Hold Time CLK-to-EN	Note 7	500			ps
t_{SKEW}	Output-to-Output Skew	Note 8			25	ps
	Part-to-Part Skew	Note 9			200	
t_{JITTER}	Cycle-to-Cycle Jitter	Note 10			1	ps_{RMS}
	Random Jitter (RJ)	Note 11			1	ps_{RMS}
	Total Jitter (TJ)	Note 12			10	ps_{PP}
	Adjacent Channel Crosstalk-induced Jitter	Note 13			0.7	$ps_{(rms)}$
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	70	140	220	ps

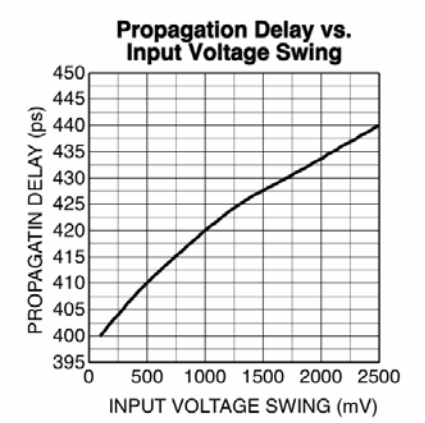
Notes:

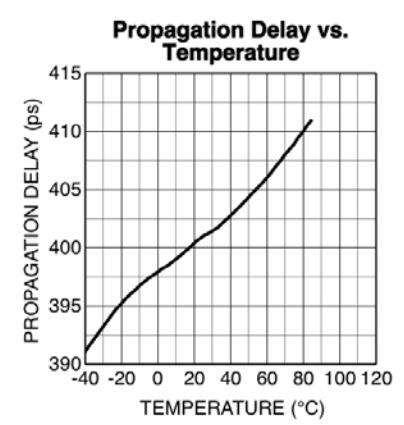
6. High-frequency AC-parameters are guaranteed by design and characterization.
7. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.
8. Output-to-output skew is measured between two different outputs under identical input transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs
10. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
11. Random jitter is measured with a K28.7 character pattern, measured at $<f_{MAX}$.
12. Total jitter definition: With an ideal clock input of frequency $<f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Operating Characteristics

V_{CC} = +3.3V, GND = 0, V_{IN} = 100mV, R_L = 50Ω to V_{CC}–2V, T_A = 25°C, unless otherwise stated.

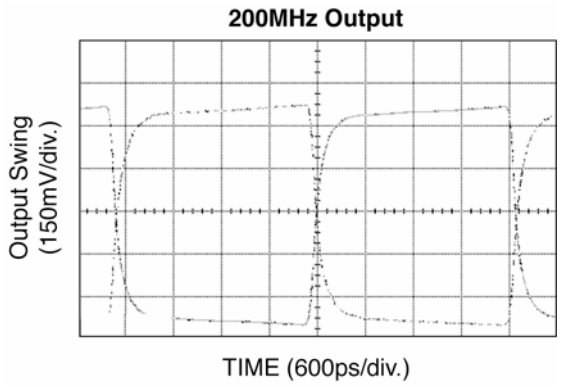


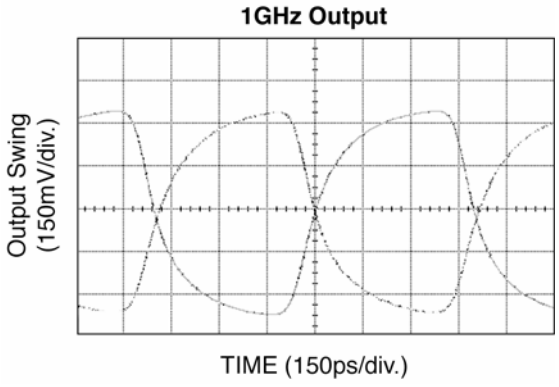


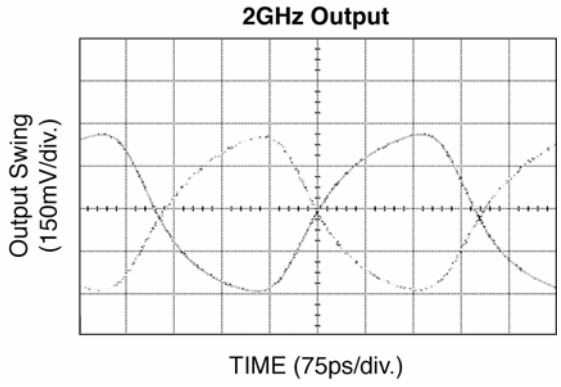


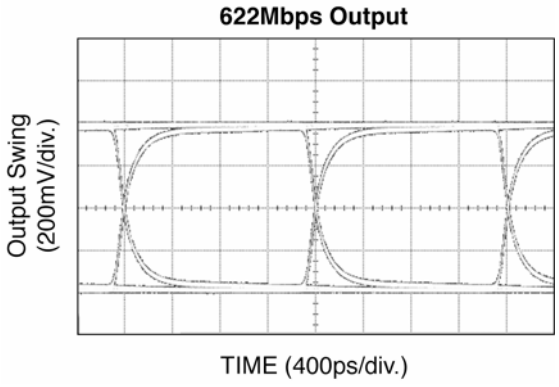
Functional Characteristics

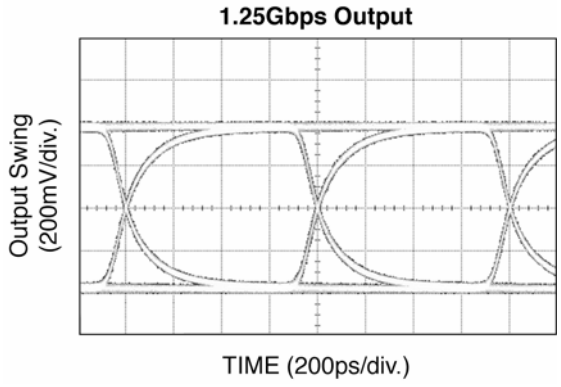
V_{CC} = +3.3V, GND = 0, V_{IN} = 100mV, R_L = 50Ω to V_{CC}–2V, T_A = 25°C, unless otherwise stated.

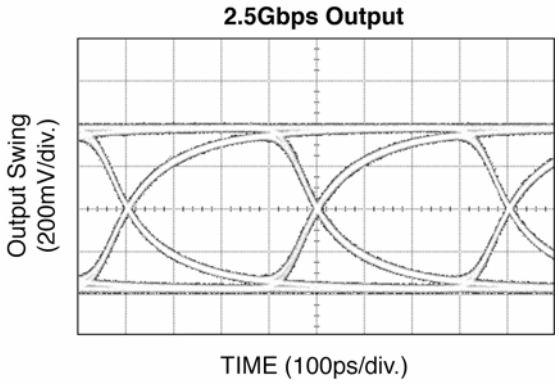












Singled-Ended and Differential Swings

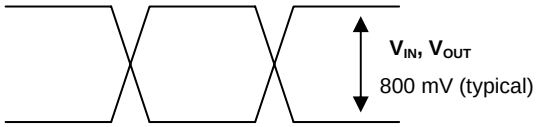


Figure 1a. Singled-Ended Voltage Swing

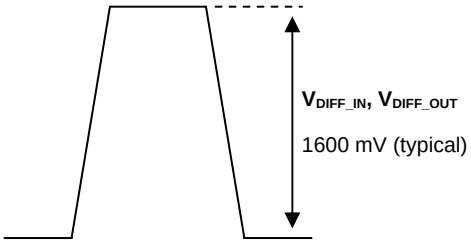
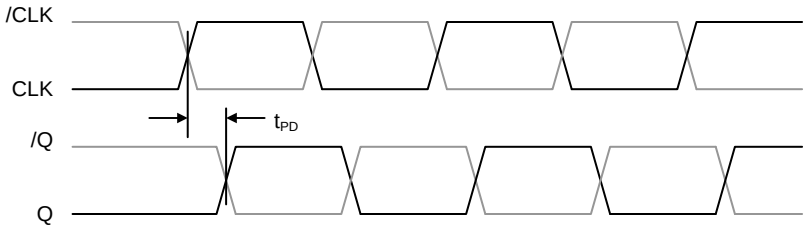
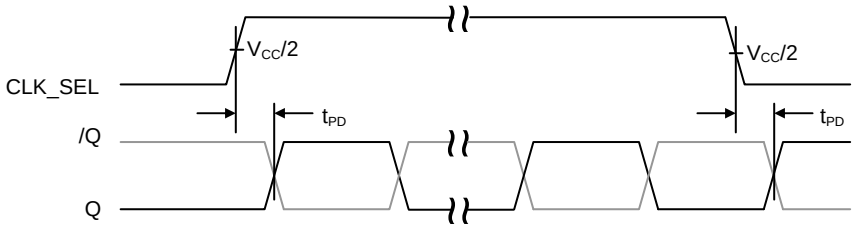


Figure1b. Differential Voltage Swing

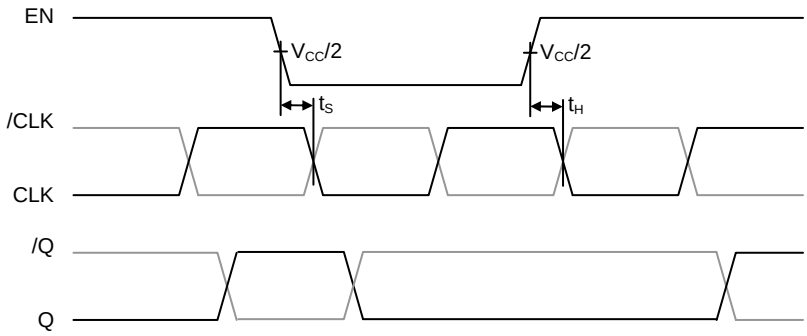
Timing Diagrams



t_{PD} – Differential In-to-Differential Out



t_{PD} – CLK_SEL-to-Differential Out



t_{PD} – Set-Up and Hold Time EN-to-Differential IN

Input and Output Stages

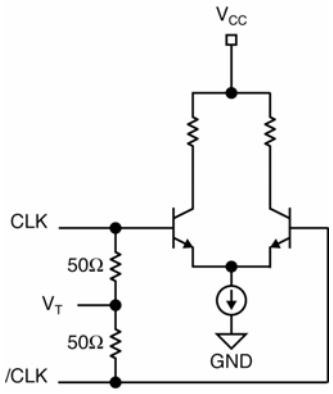


Figure 2a. Simplified Differential Input Stage

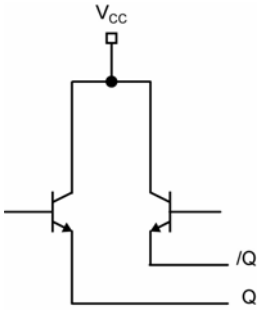


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

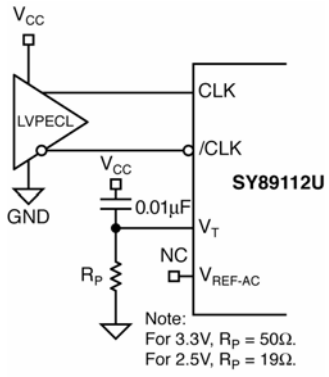


Figure 3a. LVPECL Interface (DC-Coupled)

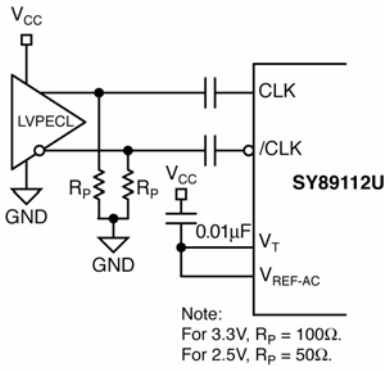
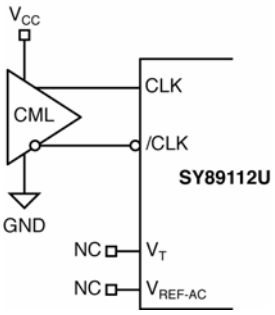


Figure 3b. LVPECL Interface (AC-Coupled)



option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

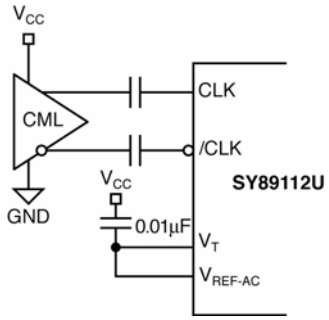


Figure 3d. CML Interface (AC-Coupled)

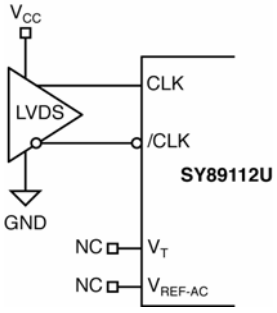


Figure 3e. LVDS Interface

LVPECL Output Interface Applications

LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing, which result in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-Resistor), and AC-Coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

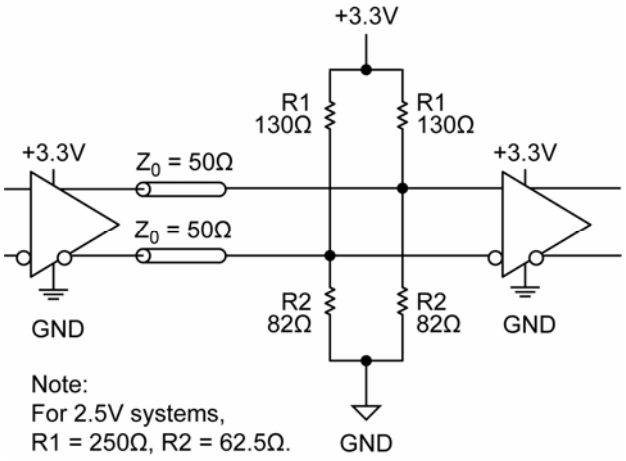


Figure 4a. Parallel Thevenin-Equivalent Termination

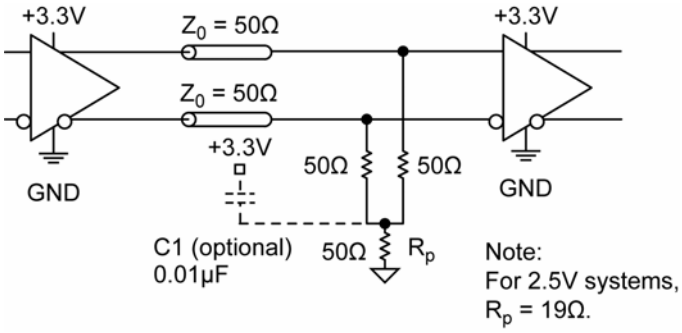
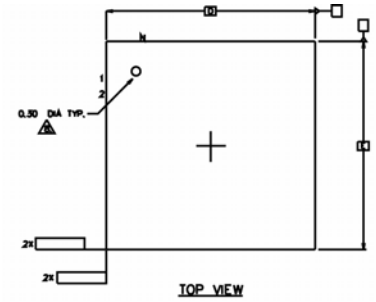


Figure 4b. Parallel Termination (3-Resistor)

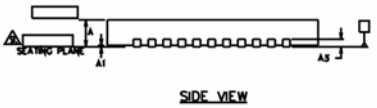
Related Product and Support Documentation

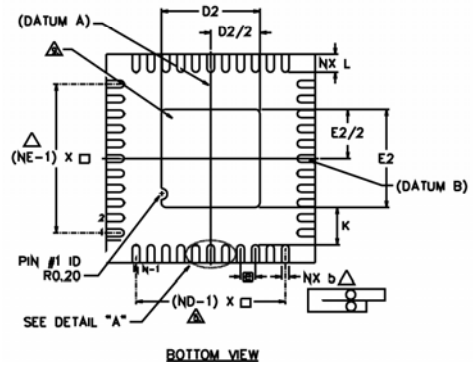
Part Number	Function	Data Sheet Link
SY89113U	2.5/3.3V Low Jitter, Low Skew 1:12 LVDS Fanout Buffer with 2:1 Input MUX and Internal Termination	http://www.micrel.com/product-info/products/sy89113u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
	MLF® Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf

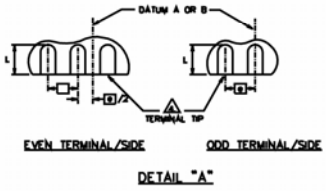
44 Lead *Micro*LeadFrame® (MLF-44)



NOTES :
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220







SYMBOL	DIMENSIONS MIN.	NOM.	MAX.	NOTE
e		0.50 BSC		
N		44		3
ND		11		6
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	—	12	2

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